Interactive Presentation Program

24th Electronics Packaging Technology Conference, EPTC 2022

Advanced Packaging

14:25 – 15:55, DEC 08 (Thur) I Waterfront Foyer

139 Inspection Solutions for Advanced IC Substrate Process Control

Park, Jong Eun[1]; Hwang, Misun[1]; Park, Chan Jin[1]; Ali, Burhan[2]; Cho, Sunki[2]; Kim, JungHyun[2]; Kim, Cheolkyu[2]
[1] *Samsung Electron-Mechanics*
[2] *Onto Innovation, Inc., Korea, Republic of (South Korea)*

224 Development of a Next Generation Stretchable Substrate for micro-LED Application

Park, Ah-Young; Lee, Jae Hak; Song, Jun-Yeob; Han, Seongheum; Kim, Seungman
Korea Institute of Machinery and Materials, Korea, Republic of (South Korea)

268 RF Performance of FOWLP to PCB Board Transition at Ka-band

Zheng, Kai Bo; Sun, Mei;Lim, Sharon Pei Siang; Jong, Ming Chinq;Lau, Boon Long;Lim, Teck Guan
*Institute of Microelectronics, A*STAR (Agency for Science, Technology and Research)*

331 TSV fabrication on a LNA SOI wafer for 3D Heterogeneous Chiplet integration

Wang, Xiangyu; Rotaru, Mihai Dragos; Yu, Haitao; Chai, Tai Chong; Chui, King Jien
Institute of microelectronics, Singapore

Advanced Optoelectronics and Displays

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276 Attachment of Alignment Fibre on Interposer for Fibre Optic Array Assembly

Wai, Leong Ching[1]; Lim, Teck Guan[1]; Chong, Ser Choong[1]; Loh, Woon Leng[2]
[1] *Institute of Microelectronics, Singapore;*
[2] *Institute of Materials Research and Engineering, Singapore*

Assembly and Manufacturing Technology

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216 Stress-less Dicing Solution for Thin Die-level Handling in 2.5D/3D IC Packaging of SOC

Park, Sunwoo[1]; Kang, Sujie[2]; Shin, YongChul[2]; Hong, Nungpyo[2]; Lee, Hyunjin[1]; Lim, Kyungbin[1]; Rhee, Minwoo[1]; Jang, Juho[2]; Oh, Jeongwon[2]; Park, Sungsoo[2]
[1] *Samsung Electronics, Korea, Republic of (South Korea);*
[2] *Joongwoo M-Tech, Korea, Republic of (South Korea)*

288 Comprehensive Study on Die Shift with Ultra-Large Embedded Multi-Die Wafer Level Packaging

Seit, Wen Wei; Chong, Ser Choong; Lim, Sharon; B G, Sajay
Institute of Microelectronics, Singapore

321 Enhancement of Vacuum Reflow Process for CCPAK - A Solution to Oxidized Lead Frame

Sanchez, Ramices Julian; Fajardo, Francis Louise Julian; Manguiat, Joshua Alcazar
Nexperia Philippines, Philippines

Electrical Simulations & Characterization

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291 Signal Integrity Analysis of IPD Decoupling Capacitor Structure

Park, Jung-Rae; Jung, Cheong-Ha; Kim, Gu-Sung
Kangnam University, Korea, Republic of (South Korea)

Emerging Technologies

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173 Evaluation of Radiopacity and Biocompatibility of Sensor Package for Smart Catheter Application

Lim, Ruiqi; Damalerio, Ramona B.; Yap, James Ven Wee; Cheng, Ming-Yuan
Institute of Microelectronics, Singapore

209 Fabrication of Cold Room Apparels with Flexible Washable Heaters

Tan, Rachel Lee Siew; Salam, Budiman; Wai, Lai Lai
Singapore Institute of Manufacturing Technology, Singapore

Interconnection Technologies

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119 Establishment of highly dense wire bonding with Insulated Au Wire

Jaafar, Norhanani; Ser Choong, Chong
Institute Of Microelectronic, Singapore

267 Introduction of Butterfly Bonding for GaN Technology

Cosme, Cristopher Agapito; Mendoza, Bongbong Aqui; Garcia, Isabel; Pascasio, Shiela
AMPLEON, Philippines

333 Process Development of Via Formation by Laser Drilling on Insulating Resin

Daniel, Ismael Cereno; Chong, Ser Choong; Hsiao, Hsiang-Yao
Institute of Microelectronics, Singapore

Thermal Management and Characterization

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176 The Effect of Porosity on Thermal Properties of Nano-Silver Solder for Electronic Packaging

Lv, Weishan; Hu, Jianxiong; Zhu, Fulong
Huazhong University of Science and Technology, China, People's Republic of

269 Thermal modelling, characteristics and optimization of 2.5D heterogeneous integrated platform for RF front end

Chen, Haoran; Lim, Teck Guan; Tang, Gongyue
*Institute of Microelectronics, A*STAR research entities, Singapore*

TSV/Wafer Level Packaging

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279 Comprehensive study on effect of chip layout and mold thickness on die shift and warpage for FOWLP applications

Lim, Sharon Pei Siang; Chong, Ser Choong; Seit, Wen Wei; Soh, Jacob Jordan; Tippabhotla, Sasi Kumar; Vempati, Srinivasa Rao
Insitute of Microelectronics, Singapore

Smart Manufacturing and Equipment Technology

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272 Automated AFM Surface Data Analysis for Wafer-to-Wafer (W2W), Chip-to-Wafer (C2W) Hybrid Bonding in Three-Dimensional Integrated Circuit (3DIC)

Chen, Jiakai; Ng, Yong Chyn; K., Mishra Dileep; Chui, K. -J.
*Institute of Microelectronics (IME), A*STAR (Agency for Science, Technology and Research)*

Interactive Presentation Program

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Materials and Processing

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115 Comparative Study of Die-Attach Materials for LED Die Bonding

Hu, Liangxing[1]; Bao, Shuyu[2]; Wang, Yue[2]; Goh, Simon Chun Kiat[3]; Lim, Yu Dian[1]; Zhao, Peng[1]; Lim, Michael Joo Zhong[1]; Miao, Weiyang[1]; Dinh, Van Quy[1]; Tan, Sai Choo[4]; Chew, Kai Hwa[4]; Tan, Chuan Seng[1,2,5]
[1] School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore;
[2] Low Energy Electronic Systems (LEES), Singapore-MIT Alliance for Research and Technology (SMART), Singapore;
[3] POET Technologies, 21 Changi North Way, Singapore;
[4] Quantum Chemical Technologies (S) Pte Ltd, 47 Pandan Road, Singapore;
*[5] Institute of Microelectronics, Agency for Science, Technology and Research (A*STAR), Singapore*

168 Effective Solderability of Water-Soluble Paste: Under Controlled Humidity of the Environment

Zhang, Ruifen
Heraeus, Singapore

171 Effects on Copper Lead-frame Oxidation by RF Plasma Process Gas Chemistry and Electrode Configuration

Toh, Johnson; Chir, Daniel
Nordson Electronics Solutions, Singapore

199 Effect of Underfill Additive Agents on Crack Prevention in Large Fan-Out Multichip Module Packages

Chen, Ching-Chia; Teng, Wen-Yu
Siliconware Precision Industries Co., Ltd., Taiwan

233 Hybrid Solder with silver hierarchical structure and particle for Synergistic effect in shear strength of die attach behaviour

Jeong, Hakyung; Lee, Jae Hak; Kim, Seung Man; Park, Ah-Young; Song, Jun-Yeob
Korea Institute of Machinery&Materials, Korea, Republic of (South Korea)

239 Diebond Process Optimization and Surface Characterization to Eliminate Conductive Die Attach Film to Ag Plated Pad Delamination due to Intrinsic High Aspect Ratio Capacitor Die Warpage and Bow Level

Pulutan, Marty Lorgino Ditaunan; Rivera, Olga
Ampleon Philippines Inc., Philippines

245 Development of Conductive Filament for 3D Circuit Printing

Kerk, Wai Tat; Tan, Yeow Meng; Tan, Lee Siew Rachel
Singapore Institute of Manufacturing Technology, Singapore

275 An efficient and innovative cleaning solution with low environmental impact

Dehon, Christophe; Lecomte, Laura; Cetier, Jonathan
Inventec Performance Chemicals, France

306 Low Temperature Silane-Based Silicon Oxides from 100°C to 300°C for Packaging Applications

Lee, Steven; Liu, Patrick; Lin, Huamao
Institute of Microelectronics, Singapore

330 Thin Memory Chip Fabrication for Multi-stack Hybrid Bonding Applications

Vasarla, Nagendra Sekhar; Mishra, Dileep K; Chong, Ser Choong; Vempati, Srinivasa Rao
*Institute of Microelectronics, A*STAR, Singapore*

Mechanical Simulation & Characterization

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132 Effect of Printed Circuit Board Design Parameters on Solder Joint Reliability for Memory Packages

Sinha, Koustav; Glancey, Christopher; Chen, Wren; Yang, Pluck; Pan, Ling; Che, Faxing; Ong, Yeow Chon; Ng, Hong Wan
Micron Technology, Inc., United States of America

204 High Density Interconnect Socket Warpage Prediction and Characterization

Ooi, Renn Chan[1]; Costa, Franco[2]; Hsieh, Sam[3]; Chiu, Ethan[3]; Xu, Wendy[4]; Yu, Dave[4]; Fan, Darwin[4]; Cheng, Allen[5]; Gattuso, Andrew[5]; Wang, Yongfu[6]; Hsieh, Currey[6]; Toran, Jeffery[7]; Thompson, John[7]; Toussaint, Pierre-Louis[8]; Curry, Ryan[9]; Loh, Wei Keat[1]; Kulterman, Ron[10]; Fu, Haley[11]

[1] Intel Corp, Malaysia; [2] Autodesk Inc.; [3] Coretech Systems Co. Ltd; [4] Celanese; [5] Foxconn Interconnect Technology; [6] Lotes Co. Ltd.; [7] Amphenol; [8] Insidix; [9] Akrometrix Inc.; [10] Flextronics Ltd.; [11] iNEMI

270 Simulation of chip placement deviation

Liu, Li; Zhang, Chunhua; Chen, Zhiwen
[1]Wuhan University of Technology
[2]Wuhan University

315 Model Validation and the Drive for Package Size Reduction

Duca, Roseanne
STMicroelectronics, Malta

Quality, Reliability & Failure Analysis

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111 Failure Analysis Case Study on Covalent Wafer bonding Delamination

Tang, Lei Jun; Jasmine, Woo; Michelle, Chew; Kenneth, Lee; Chi, Ting Ta
Institute of Microelectronics, Singapore

125 Fault Isolation for Board-Level Solder Joint Failure Using Time-Domain Reflectometry

Chen, Yi-Yu; Liu, Wen-Ju; Zou, Yung-Sheng; Chung, Min-Hua; Gan, Chong-Leong; Takiar, Hem
Micron Technology, Inc., Taiwan

126 Fatigue performance of Cu/Sn–3.0Ag–0.5Cu/Cu solder joints at different current densities

Liu, Longgen; Wang, Bo; Li, Wangyun; Gong, Yubing; Pan, kailin
School of Mechanical and Electrical Engineering, Guilin University of Electronic Technology, Guilin, 541004, China

140 Studies of Electron Backscattered Diffraction (EBSD) Analysis Technique and Its Applications in Wafer Fabrication and Advanced Packaging

Hua, Younan; Liao, Lois
Wintech-nano, Singapore

201 EOS-induced failure analysis of FPGAs

HUANG, Yan; JIANG, Panpan; LIU, Tianhan; LIANG, Chaohui
No.5 Electronics Research Institute of the Ministry of Industry and Information Technology, Guangzhou, 511370, P.R. China